Full ISBUS Signals

"A" Side Connectors

1A NIOREQ I/O Request (TTL Level Output from CPU/Controller)

Input/Output request line. Active low. Indicates that the address bus lines AB0 to AB7 hold a valid address for an I/O access. (During an interrupt acknowledge cycle, and only then, NIORQ is produced at the same time as NM1(OCF); at all other times NM1(OCF) is produced together with NMREQ or NEMREQ, never with NIOREQ.)

The 8 address bits define which one of 256 ports are to be accessed. Future systems may have a larger I/O port space, and to prevent these ports conflicting with the existing 256 ports NIOREQ will be denied to the bus; instead an "extended I/O request" signal will be produced.

2A NMREQ Memory Request (TTL Level Output from CPU/Controller)

Memory request line, active low; indicates that the 16-bit address bus, AB0-AB15, holds a valid address for a memory access, ie an access to one of the first 64K memory addresses is in progress.

Future systems will have a further 8 address lines (AB16-AB23), defining a 16 Megabyte memory space. To prevent the addresses in the larger space conflicting with the existing 64K space NMREQ will be denied to the bus; instead an "extended memory request" signal will be produced.

3A NWDS Write Data Strobe (TTL Level Output from CPU/Controller)

Write line, active low. Indicates that the data bus has valid data to be written to a memory location or output to an I/O device.

4A NRDS Read Data Strobe (TTL Level Output from CPU/Controller)

Read Line, active low. Indicates that the CPU/Controller wants to read data from a memory location or I/O device.

5A-20A AB15-AB0 16-bit Address Bus (TTL Level Outputs from CPU/Controller)

These are the address lines for a normal memory access (ie when NMREQ or NEMREQ are present). The positive logic convention is used, i.e. a "0" is represented by a low voltage and a "1" by a more postive voltage. The address lines are usually driven from the CPU, but if the CPU card can be rendered high impedance (disabled) these lines can be driven from other controllers (e.g. Direct Memory

Access (DMA) devices). In ISBUS "A" systems these 16 are all that are used , but in ISBUS "B" systems there are a further 8 lines (AB16-AB23) defined for addresses.

When the access is to the I/O space (ie when NIOREQ or NEIOREQ are present) the lower 8 lines, AB7-AB0, carry the address of the I/O port being accessed and the other lines carry information which depends on the particular microprocessor in use.

A final use of the address bus is to carry a "refresh address" for dynamic RAMs. This is issued at a time when the MPU is not using the bus (ie immediately after an opcode fetch, while the instruction the opcode represents is being decoded) and allows an easy refresh of dynamic RAMs. The indication that the address bus bears a refresh address is provided by the NRFSH signal. NMREQ and/or NEMREQ are also present but NRDS and NWDS are denied so that an actual memory access does not take place. As a result it is possible therefore to refresh an unlimited quantity of memory cards at once, with the same refresh signals. (The refresh address was originally produced by the Z80-CPU itself, but as it is only 7 bits, (ie AB0-AB6) it is likely that some modification will be required to the refresh arrangements if 256K DRAM chips are used (since these need more than a 7 bits refresh).)

21A NRST System Reset (Open Collector to or from CPU/Controller)

This signal is active (ie low) when the reset switch on the CPU card is reset. It is used to reset circuitry on all of the cards in the system which require such a signal. If the reset line is brought low by the action of a device other than the CPU then the CPU is also reset. The line is normally held high by a 1k pull-up resistor on the CPU card.

(The Kemitron MZB-3 CPU card does not comply with this specification in all details.)

So as not to run the risk of damage to data in the dynamic RAMs when the reset switch is operated, the CPU card produces a short duration pulse rather than a permanent signal for the duration of the reset switch operation. Furthermore the start of the pulsed refresh is arranged to be never during a memory access (because an incompleted access could corrupt a row of data in a dynamic RAM).

Full ISBUS Signals

22A-29A DB7-DB0 8-bit Data Bus (Bidirectional, 3-state)

These are the data lines used for 8-bit bidirectional data exchanges between the CPU or Controller and Memory or Input/Output Cards. Positive logic is used (as for the address lines previously described). In 8-bit systems these 8 lines are the only 8, but for systems using a 16-bit bus there are a further 8 lines defined on the "B" side of the bus.

30A (Unallocated) Daisy Chain 1 In (Daisy Chain TTL Level Input)
31A (Unallocated) Daisy Chain 1 Out (Daisy Chain TTL Level Output)

These two lines allow an additional and as yet unallocated priority daisy chain to be set up. Viewed from the plug in card side of the edge connector, the output of the card on the left is connected to the input of the card on the right. The convention used will be active low.

32A NRFSH DRAM Refresh (TTL Level Output from CPU/Controller)

Refresh line, active low, indicates that the lower address bus lines (at least the seven lines AB0-AB6, but may be more) hold a refresh address for dynamic RAMs. It is the duty of the CPU or Controller card to ensure that refresh addresses are issued frequently enough for proper refresh of dynamic RAMs in the system. If the dynamic RAM card in use has its own refresh counter the CPU or Controller is relieved of this duty; the NRFSH signal can then merely be used to signal to the dynamic RAM card that now is an appropriate time for a refresh to take place.

33A Ø MPU Clock (TTL Level Output from CPU/Controller)

This is the single phase system clock (often 2.5 MHz for a standard Z80-CPU, 4 MHz for the "A" version, 6 MHz for the "B" version and 7.5 MHz for the "H" version). Ø is derived from the 2 x MPU clock to be found at pin 34B of the ISBUS. Ø changes state on the negative transition of 2Ø. The buffering on the CPU card should be organised so that the bus clocks Ø and 2Ø are one buffer delay in advance of the CPU clock itself. This is because (in the case of a Z80 system) many of the family peripheral chips cannot accept a TTL Level clock: its voltage swing and current drive have to be amplified first, which adds an extra buffer delay.

Full ISBUS Signals

34A NWAIT   Wait State Request (Open Collector Input to CPU/Controller)

This signal, if active (ie low) during the Z80 "T2" time, indicates that an addressed device requires "wait" states to be inserted into the current Memory or I/O cycle. This is usually to accommodate slow devices which require an increased time before data can be provided or taken, but another use for "wait" states is to allow synchronisation between the CPU and the Memory or I/O device if timing is critical (e.g. for some floppy disk controllers, or VDU designs). If the CPU is providing dynamic RAM refresh, prolonged use of "wait" states should be avoided as it may predjudice proper refreshing of the dynamic RAM. (There is no need to panic on this point - the maximum wait state allowed can be calculated fairly easily for specific cases.) A 1k pull-up resistor is fitted on the CPU card.

35A +12V   +12V Power Supply Rail
36A +12V   +12V Power Supply Rail

Together with their "opposite numbers" 35B and 36B on the other side of the connector, these are the conductors of +12V regulated d.c. power from the power supply to the system. Generally these rails carry no more than an Ampere or two, and if this is the case there is no need to reinforce the copper track on the bus board.

37A Pol   Polarisation Slot

This line is not available for signals as this position is removed for polarisation. An important secondary purpose for the polarisation key fitted in each connector at this position is to pull the cards into line - to prevent individual connectors shorting between adjacent contacts.

38A -12V   -12V Power Supply Rail
39A -12V   -12V Power Supply Rail

Together with 38B and 39B on the other side of the connector, these are the conductors of -12V regulated d.c. power from the power supply to the system. Generally these rails carry much less than an Ampere, and if so there is no need to reinforce the copper track on the bus board.

40A 0V 0V Power Supply Rail
41A 0V 0V Power Supply Rail

Together with 40B and 41B on the other side of the connector, these provide the return path to 0V and Earth for the currents flowing in the +12V, +5V and -12V rails. Usually the algebraic sum of these currents is more than the absolute value of any one of them, so these rails carry most current of all. If the current is substantial, say 10 Amperes or more, it may be advisable to reinforce these rails with lengths of heavy gauge tinned copper wire e.g. 18 swg. This is quite easy to do because the wire can lie between the two adjacent rails provided for this voltage on each side of the connector.

42A +5V +5V Power Supply Rail
43A +5V +5V Power Supply Rail

Together with 42B and 43B on the other side of the connector, these are the conductors of +5V regulated d.c. power from the power supply to the system. If the current drawn from this rail is substantial, say approaching 10 Amperes or more, it may be advisable to reinforce these rails with lengths of heavy gauge tinned copper wire e.g. 18 swg. This is quite easy to do because the wire can lie between the two adjacent rails provided for this voltage on each side of the connector.

This concludes the description of the signals on the "A" side of the ISBUS. These are all that have been used so far and alone they permit a very powerful system (which has stood the test of time) to be implemented. However as developments in computers proceed there may come a time when even more capability is required. The as yet unused "B" side connectors have been provided for future enhancements which therefore will be possible without the need to scrap all that has been built so far. If the Interak system is compared with its contemporaries (ie systems designed 5 or 6 years ago) it will be seen how far-sighted this approach has been. The vast majority of earlier computers have had to be scrapped once the limits of 8 bits and 64K have been reached, and it is intended that this will not be the fate of the Interak system.

The following pages describe these extra "B" side signals.

Full ISBUS Signals

"B" Side Connectors

1B NEIOREQ Extended I/O Request (TTL Level Output from CPU/Controller)

This is an active low signal which is only used in systems with a 64K I/O space (i.e. 16-bit Port Address Bus). It has a similar function to the NIOREQ line on 1A of the bus, but NEIOREQ is only issued when the extended port space is brought into play.

2B NEMREQ Extended Memory Request (TTL Level Output from CPU/Controller)

This is a signal (active low) which is only used in systems with a 16 Megabyte Memory Space (i.e. 24-bit Address Bus). It has a similar function to the NMREQ line on 1B of the bus, but NEMREQ is only issued when the extended address space is to be used.

3B NADS Address Strobe (TTL Level Output from CPU/Controller)

This is an active low signal which has been allocated for future use. Once 32-bit (and beyond?) CPUs are introduced, the idea of separate address and data buses (i.e. 32+32=64 bits) becomes unwieldy; it is possible that the normal implementation will be to use a multiplexed address-data bus. As ISBUS has 16 data bus lines defined, and 24 address bus lines, i.e. 16+24 = 40 lines in total this will be more than enough for 32-bits. When this happens, an extra strobe will be required: NADS, which indicates that the address-data bus holds a 32-bit address. When NADS is over the bus will then be driven with the data corresponding to that address.

The possibility of non-multiplexed 32-bit address and data buses has not been ruled out, but if they are introduced this will need very extensive alterations to the bus signals. Indeed so much will have to change that the user may then have to say goodbye to the old cards forever. A better idea in our view, if a lot of investment has been made in non 64 address and data bit systems, is that then more than one CPU be run simultaneously, on separate buses, sharing the computational load between each other.

4B NDIRIN Direction In (to MPU) (TTL Level Output from CPU/Controller)

It is very convenient for setting buffer directions if the CPU/Controller card issues a direction signal early in its cycle. Most current CPUs do not issue such a signal, but if in the future CPUs etc. are used which do, this bus line has been allocated to carry it. It is an active low signal.

Full ISBUS Signals

5B NM1(OCF) M1 (Opcode Fetch) (TTL Level Output from CPU/Controller)

This is the M1 signal from the Z80 CPU. It is used to indicate that the CPU is fetching an op-code. (M1 is also asserted by the CPU with IORQ during the special conditions of an interrupt acknowledge cycle.)

6B (Unallocated) Extended Signal 1 (TTL Level Output from CPU/Controller)
7B (Unallocated) Extended Signal 2 (TTL Level Output from CPU/Controller)

Although it is an irritating feature of a bus standard to have unallocated lines, these are so at present. They should not be employed for the user's own purposes, as this may conflict with whatever signal is allocated to them in the future. If they carry control signals the signals will be active low.

8B NZCMAINS Zero Crossing (Mains) (TTL Level Output from CPU/Controller)

This signal is a series of short pulses (active low), synchronised with the zero crossings of the ac mains input to the computer. It has three main purposes - firstly for triggering ac power controlling devices and the like (so that ac powered circuits can be switched on only when the mains voltage is passing through zero thus avoiding current surges and unwanted generation of electromagnetic interference) - secondly to provide advance warning of an imminent power failure (since when the ac mains fails there will be a period of continuous "zero crossing" before dc power fails) - and finally to offer a simple timing pulse of known repetition frequency which is independent of any software (this can be used for example to set a "watchdog" timer to alert of or restart a "looping" or "crashed" program).

9B NNMI Non Maskable Interrupt (Open Collector to or from CPU/Controller)

Active low, non-maskable interrupt line. 1k pull-up resistor fitted on the CPU card.

10B NINTA Interrupt A (Open Collector to or from CPU/Controller)

Active low, maskable interrupt line, 1K pull-up resistor fitted on the CPU card.

11B NINTB   Interrupt B   (Open Collector to or from CPU/Controller)

This is a further active low line similar in function to Interrupt A and is provided for any future CPUs which can use an extra interrupt line.

12B NINTC   Interrupt C   (Open Collector to or from CPU/Controller)

This is a further active low line similar in function to Interrupt A and is provided for any future CPUs which can use an extra interrupt line.

13B-20B   AB16-AB23   Extended Address Bus (TTL Level Output from CPU/Controller)

These provide an extra 8 positive logic address lines to extend the memory space memory space to 16 Megabytes. The extra lines are produced by the CPU/Controller card. When these lines are used in a system the NEMREQ (Extended Memory Request) signal replaces the ordinary NMREQ signal of a non-extended (64K) system, to prevent any conflict where the old 64K system memory space is shared with the new 16 Megabyte system.

21B NBUSREQ Bus Request   (Open Collector Input to CPU/Controller)

This is an active low signal which is output by some card (e.g. Direct Memory Access Controller) to request the existing controller (e.g. CPU card) to relinquish its control of the bus. Most of the bus output lines from the existing controller are allowed to go tri-state, and it then generates the signal NBUSAK (q.v.) Care must be taken when using this technique to ensure that arrangements for dynamic RAM refresh (for example) are properly made if the CPU card is effectively switched off.

(At the time of writing no decision has been taken on whether or not the clock signals generated by the CPU card should also be rendered tri-state, and replaced by ones from the DMA controller, also the question of what effect interrupts should have is likewise very vague.)

Full ISBUS Signals

22B-29B DB15-DB8 Extended Data Bus (Bidirectional, 3-state)

When systems require a 16-bit data bus, these lines carry the upper 8-bits of that data. They are directly opposite the bus lines for the lower 8-bits and this enables easy conversion of existing 8-bit cards to use the uppper 8-bits instead, so that cards can be used in pairs to provide an easy upgrade to 16-bits. The positive logic convention is used, as described for the address lines on the "A" side.

30B NIEI Interrupt A Daisy In (Daisy Chain TTL Level Input)
31B NIEO Interrupt A Daisy Out (Daisy Chain TTL Level Output)

These active low signals are used by Z80 peripherals to form an interrupt daisy-chain for determination of interrupt priority. This is done in accordance with the rules set out by the manufacturers of the chips to be used.

32B NBAI Bus Available Daisy In (Daisy Chain TTL Level Input)

This active low signal forms a daisy chain with NBAO (below). The action is for a slave device/channel controller not to start an access if this line is high.

33B NBAO Bus Available Daisy Out (Daisy Chain TTL Level Output)

This active low signal forms a daisy chain with BAI. It is set low by e.g. the CPU card when the CPU has received a request from say a Direct Memory Access controller to release the system bus. NBAO is high when the bus is being used.

Because it is part of a daisy chain, the physical order of the cards using it will determine their priority to access the bus.

34B 20 2 x MPU Clock (TTL Level Output from CPU/Controller)

This is a clock of twice the frequency of that on bus line 33A (and thus is often 5 MHz for a standard Z80-CPU, 8 MHz for the "A" version, 12 MHz for the "B" version and 15 MHz for the "H" version). 0 on pin 33A is derived from this clock; 0 changes state on the negative transition of 20. The buffering on the CPU card should be organised so that the bus clocks 0 and 20 are one buffer delay in advance of the CPU clock itself. This is because (in a Z80 system) many of the family peripheral chips cannot accept a TTL Level clock: its voltage swing and current drive have to be amplified first, which adds an extra buffer delay.

35B +12V   +12V Power Supply Rail
36B +12V   +12V Power Supply Rail

These are connected to the same +12V Power Supply Rail as described for connections 35A and 36A on the "A" side of the connector.

37B Pol   Polarisation Slot -

This line is not available for signals as this position is removed for polarisation. Also it is used with the key fitted in each connector to pull the cards into line and prevent individual connectors shorting between adjacent contacts.

38B -12V   -12V Power Supply Rail
39B -12V   -12V Power Supply Rail

These are connected to the -12V Power Supply Rail - see the description for connections 38A and 39A on the "A" side.

40B 0V   0V Power Supply Rail
41B 0V   0V Power Supply Rail

The 0V Rail is on these two pins, and the 40A and 41A on the "A" side. See the description for 40A and 41B for full details.

42B +5V   +5V Power Supply Rail
43B +5V   +5V Power Supply Rail

These, and 42A and 43A on the other side of the connector form the +5V Power Supply Rail. See the description for 42A and 42B for more information.

Derived Signal

NINTAK: This signal indicates that the CPU is acknowledging an interrupt and expects an interrupt vector to be placed on the data bus.

The NINTAK signal can be produced as the output of an "OR" gate (e.g. 74LS32) which has NIOREQ and NM1(OCF) connected to its inputs. As it can be produced in this way anywhere it is needed there is no need to allocate a bus line to it.